ARCHIVES	O F	METALLURGY	AND	MATERIALS
Volume 51	ELL 我不会是今天中国日	2006		Trave 4

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TEM STUDY OF IRIDIUM SILICIDE CONTACT LAYERS FOR LOW SCHOTTKY BARRIER MOSFETS

BADANIA PRZY UŻYCIU TEM WARSTW KONTAKTOWYCH Z KRZEMKU IRYDU STOSOWANYCH W TRANZYSTORAC TYPU MOSFET Z NISKĄ BARIERĄ SCHOTKKY'EGO

An influence of annealing temperatures (300, 400 and 500°C) on the iridium silicide formation in the Ir/Si structure was analysed by means of the transmission electron microscopy (TEM). The silicide layer is formed by the solid-state reaction between 15 nm thick Ir metallisation and a Si layer during the rapid-thermal-annealing (RTA) process for 120 s. The silicide layers are used as source/drain contacts for a novel technology of low Schottky barrier MOSFETs on SOI. For this reason the high quality of the silicide/Si interface and the silicide structure are essential for the electrical properties of the device. The studies enabled the determination of the silicide layer thickness, the layer morphology, and the silicide/Si interface roughness as well as the identification of the silicide phase. Annealing of the Ir/Si structure at 300 and 400°C caused formation of an amorphous iridium silicide layer between the iridium layer and the silicon substrate. At the highest annealing temperature (500°C) the whole Ir layer completely reacted with Si, forming a crystalline iridium silicide layer. A diffraction analysis showed that the silicide layer consists of the dominant IrSi orthorhombic phase and another silicide phase with higher content of silicon (IrSix). The IrSix is placed between IrSi and Si. It indicates that during solid-state reaction at 500°C the Si diffusion is predominant.

Keywords: annealing, iridium silicide, selected-area diffraction, transmission electron microscope

Wpływ różnych temperatur wygrzewania (300, 400 i 500°C) na proces tworzenia się krzemku irydu w strukturze Ir/Si był badany za pomocą transmisyjnej mikroskopii elektronowej (TEM). Warstwa krzemkowa tworzy się podczas wygrzewania przez 120 s metodą RTA 15 nm warstwy irydu osadzonej na podłożu krzemowym. Tak wytworzone warstwy krzemkowe stosowane są jako źrodło/dren kontakty w nowoczesnej technologii tranzystorów typu MOSFET na podłożach SOI. Uzyskanie najlepszych parametrów elektrycznych tranzystorów zależy od struktury krzemku jak i bardzo gładkiej granicy fazowej krzemek/Si. Badania przy użyciu TEM polegają na określeniu grubości i morfologii warstw krzemkowych, gładkości granicy fazowej krzemek/Si, jak również ustaleniu rodzaju struktury krystalicznej tworzącego się krzemku irydu. Wygrzewanie struktury w temperaturze 300 i 400°C powoduje tworzenie się amorficznej warstwy krzemku irydu pomiędzy warstwą irydu a podłożem krzemowym. W najwyższej temperaturze wygrzewania (500°C) cała warstwa irydu reaguje z krzemem, tworząc krystaliczną warstwę krzemku irydu. Analiza dyfrakcyjna wykazała, że warstwa krzemkowa składa się z dominującej fazy IrSi o budowie rombowej oraz innej fazy krzemku irydu zawierającej więcej krzemu (IrSix) i położonej pomiędzy fazą IrSi a podłożem krzemowym. Wynik ten wskazuje, że podczas reakcji w 500°C dyfuzja Si jest dominująca.

1. Introduction

Due to interesting properties of the metal-silicides such as the thermal stability, the low resistivity, and the reduced silicide/silicon specific contact resistance, metal-silicide layers have been applied as source/drain (S/D) contacts in low Schottky barrier MOSFETs [1]. This novel technology demonstrates the advantage of low Schottky S/D over conventional technologies of implanted S/D, because it is easier to manufacture due to

avoiding the use of highly doped S/D regions. Iridium silicide is a very promising candidate for S/D contacts [2]. It demonstrates among various silicides the lowest Schottky barrier for holes [3], and is potentially even more attractive than widely applied PtSi-based contacts [1-4].

Issue 4

Generally, a metal deposited on Si and by subsequently annealed forms a metal-silicide. Solid-state reaction occurs by interdiffusion of metal and silicon atoms at a metal/silicon interface. During the growth of the

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metal-silicides the supply of either metal or silicon atoms dominates [5]. In case of the iridium silicide growth, when a few nanometres of the Ir film is deposited at the room-temperature (RT), diffusion of Ir atoms into the Si substrate is predominant and in turn during annealing at 500°C of room-temperature deposited iridium on silicon, Si diffusion into the polycrystalline Ir film is predominant [6].

Petersson [7] reported that annealing of iridium deposited on silicon formed three different phases: IrSi, IrSi_{1.75} and IrSi₃ at temperature ranges: 400-600°C, 500-950°C and 1000°C, respectively. Other compositions of the iridium silicide phase such as Ir_3Si_5 and epitaxial Ir_3Si_4 formed by deposition of Ir film on Si(100) under ultrahigh vacuum conditions have been found by Engström et al. [8] and by Chung et al. [9], respectively.

The various iridium silicides show different Schottky barrier heights on Si [6,10-12]. The difference in Schottky barrier heights may be attributed to the merged effect of phase composition and microstructure difference between various phases of iridium silicide [12]. Also, a very important issue is the influence of the Schottky-contact microstructure on the electrical properties of the contact.

The transmission electron microscopy (TEM) investigations are very helpful for the technology optimalization and the understanding the Schottky-contact electrical performance. In this paper, an influence of annealing temperatures (300, 400 and 500°C) on the iridium silicide formation in the Ir/Si structure is analysed by means of the TEM. The studies enabled the determination of the silicide layer thickness, the layer morphology, and the silicide/Si interface roughness as well as the identification of the silicide phase. In our previous work [13] the iridium silicide formation process after annealing at 300, 600 and 900°C was studied. The reaction at 600 and 900°C was very intensive and produced silicide layers of a very low quality. The best electrical performance was obtained at 300°C for which TEM analysis reveals a continuous and regular layer of iridium silicide. One could expect that in the temperature range from 300 to 500°C thermally stable iridium silicide contact layers can be formed. The silicide layers formed in this temperature range exhibit good electrical performance.

2. Experimental

The iridium-silicide contact layer was formed by the e-gun evaporation of a 15 nm thick Ir layer on a *p*-type Si(100) substrate (with the boron concentration 1.5×10^{16} cm⁻³) and subsequently annealed for 120 s by the rapid-thermal-annealing (RTA) process at various temperatures: 300, 400 and 500°C. The formation process of the iridium silicide was investigated by means of cross-sectional transmission electron microscopy (XTEM). Specimens were prepared by the method described in Ref. [14] and studied in the JEM-200CX transmission electron microscope operating at 200 kV. TEM electron diffraction techniques were used to identify the silicide phases.

3. Results and discussion

The XTEM micrographs revealed that after annealing of the Ir/Si contact structure at 300 (Fig. 1a) and 400°C (Fig. 1b) between the iridium layer and the silicon substrate an amorphous Ir-Si layer was formed. The thickness of the newly formed silicide layer is about 5 and 7 nm after annealing at 300 and 400°C, respectively. The grains in the Ir layer for both annealing temperatures have various shapes and some of them are columnar and regular. These grains are big enough to form the layer as a single layer of the iridium grains placed side by side. The selected-area diffraction patterns (SADP) from the Ir/Ir-Si/Si region after annealing of the Ir/Si sample at 300 and 400°C are showed in Fig. 1c and d, respectively. The lack of reflections corresponding to other phases than iridium in the electron diffraction patterns, clearly demonstrates that the remaining iridium layer is homogenous. The thickness of the unreacted Ir layer is about 12-13 nm and about 11 nm for the sample annealed at 300 and 400°C, respectively. After annealing the Ir/Ir-Si/Si interfaces are smooth, but the top surface of the Ir layer in both cases is rough (Fig. 1a and b).



Fig. 1. TEM cross-sections of the Ir/Si microstructure annealed at: (a) 300°C or (b) 400°C and corresponding electron diffraction patterns at: (c) 300°C or (d) 400°C. [011]-orientated Si reflections (marked by the white-dashed lines) and poly-rings from unreacted Ir layer (with superimposed white lines) are revealed in electron diffraction patterns



Fig. 2. A TEM cross-section of the Ir/Si structure annealed at 500°C: (a) cross-sectional view and (b) electron diffraction pattern of the structure. [001]-orientated Si reflections (marked by the white-dashed lines) and poly-rings of the IrSi orthorhombic phase (marked by the white lines) are revealed in the electron diffraction pattern

The XTEM micrograph revealed that after annealing of the Ir/Si contact structure at 500°C (Fig. 2a) all the Ir atoms from the initially deposited layer reacted with silicon. In consequence a crystalline iridium silicide layer was formed. The thickness of this layer is about 28-30 nm, however the Ir layer before reaction was only 15 nm thick. It demonstrated that the ratio of the iridium silicide layer thickness to the initial iridium layer thickness is very close to two. Irregular grains were visible in this layer. The top surface of the iridium silicide layer is rough similarly as the top surface of the Ir layer at lower annealing temperatures (300 and 400°C). The silicide/Si interface is slightly rough. It can be observed that the silicide layer consists of two phases (Fig. 2b). The thickness of the upper phase equals to about 21-23 nm and of the phase located below about 7 nm. The continuity of the bottom phase in certain areas is broken by the grains of the thicker phase, which grew up to the silicon substrate (Fig. 2a). An analysis of the electron diffraction pattern revealed clear polycrystalline rings corresponding to the IrSi orthorhombic phase [15] and some unidentified reflections (marked by black lines in Fig. 2b) placed in the vicinity of the (101)IrSi line ($d_{(101)} =$

0,415 nm), which can correspond to the IrSi_x phase. A precise identification of the IrSix phase is difficult due to small size of IrSix grains only few reflections in the electron diffraction pattern can be found. However, it can be noticed, that unidentified reflections are close to some lines corresponding to the IrSi1.5 monoclinic phase (see Table III in [7]) or can correspond to another silicide phase with higher content of silicon, but certainly not belonging to the IrSi1.75 monoclinic phase described also by Petersson [7]. Ohdomari [10] reported that the 20 nm thick Ir film completely reacted with silicon during the annealing at 500°C for 1 h. The final reaction forms IrSi and a very small amount of the Ir₂Si₃ (i.e. IrSi_{1.5}) phase located between IrSi and Si. This result can confirm our conjecture that IrSi15 phase can be formed in samples annealed at 500°C. Petersson [7] described an occurrence of the IrSi_{1.75} phase after annealing at 500°C, but only after long annealing time of many hours. It explains the absence of the IrSi_{1.75} phase in our sample annealed at 500°C by RTA for 120 s. The formation of an amorphous silicide layer in the first stage of the solid-state reaction is caused by a negative enthalpy of metal and silicon atoms mixing in the amorphous phase [16-20]. The amorphous layer grows to a maximum thickness (depending on conditions of the formation process) and then transforms to the polycrystalline silicide layer. Demuth et al. [6] reported that the 3-7 nm thick amorphous iridium layer is formed between the as-deposited 60 nm thick Ir film (deposited in an UHV conditions) and the Si substrate. They have also observed formation of the 6-7 nm thick amorphous iridium silicide layer after heating at 500°C for 30 s of the Ir film (60 nm) deposited on a silicon substrate. A similar result was obtained in our work. The thickness of the amorphous iridium silicide layer, which was formed in the sample annealed at 400°C equals 7 nm. It proves that the maximum thickness of the growing amorphous iridium silicide layer reaches several nanometres. However, in the experiment carried out by Ohdomari [10] a partial interface reaction occurred after annealing at 300 and 400°C for 1h, where about 30% of Ir transformed to crystalline IrSi. The lack of the formation of an amorphous iridium silicide layer can be explained by longer time of annealing (1 h). One conclusion can be drawn from it that beside the annealing temperature also the annealing time has an influence on a form of the silicide (i.e. the amorphous, the crystalline or a mixture of both). When the annealing is prolonged the crystalline phase nucleates and consumes the amorphous phase. It was mentioned that RTA annealing at 500°C for 30 s does not produce yet a crystalline iridium silicide layer while annealing at 500°C for 30 min (with also 60 nm thick Ir film deposited on Si) produces a silicide layer with amorphous and crystalline regions

[6]. In our case annealing at 500°C for 120 s (with 15 nm thick initial Ir layer) is sufficient for the formation of the crystalline iridium silicide layer, which consists of IrSi and $IrSi_x$ phases. The IrSi_x phase, which supposedly is IrSi_{1.5} monoclinic phase (although it is not fully confirmed), contains more of silicon than IrSi and is placed between IrSi and Si. It confirms the reported suggestion in [6] that during solid-state reaction at 500°C the Si diffusion is predominant.

4. Conclusions

The formation of the iridium silicide in the Ir/Si structure was studied by means of TEM. Annealing at 300 and 400°C for 120 s causes only a partial reaction between Ir and Si and the formation of the amorphous iridium silicide layer at the Ir/Si interface. At the highest annealing temperatures (500°C) the reaction is fully completed and forms the crystalline silicide layer that consists of two phases. Electron diffraction analysis confirmed an existence in the silicide layer of the dominant IrSi orthorhombic phase and IrSi_x (x>1) phase. The formation of the silicide phase containing higher content of silicon between IrSi and Si substrate indicates that the Si diffusion is predominant at 500°C.

Acknowledgements

This publication is based on the research partly supported by the European Commission under the project "Metallic Source/Drain Architecture for Advanced MOS Technology" (IST-016677 META-MOS).

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Received: 20 September 2006.

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