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BARRIER INHOMOGENEITY OF PT/GAN JUNCTIONS WITH A LOW-TEMPERATURE ALD GROWN ZnO INTERLAYER

Semiconducting GaN can realize high performance electronic and power devices owing to its high electron mobility and thermal conductivity where good metal-semiconductor contact is prerequisite. In this work, using thermal atomic layer deposition (ALD), ZnO interlayer was grown at 80°C on GaN and the Pt/ZnO/GaN heterojunctions were electrically characterized. The analyses on the current–voltage (*I–V*) and capacitance (*C–V*) data showed that the forward *I–V* conduction was involved with the inhomogeneous Schottky barrier. The higher density of interface states from *I–V* data than that from *C–V* data was attributed to nonuniform distribution of interface states. In addition, high density of interface states caused localized high electric field, caused higher Poole Frenkel emission coefficients than the theoretical one.

Keywords: ZnO interlayer; GaN; Inhomogeneous Schottky barrier; Interface states

1. Introduction

GaN has been applied for various devices because of its good intrinsic properties of electron saturation drift velocity, breakdown field, and thermal conductivity [1-3]. To realize high-performance GaN-based devices, metal-semiconductor (MS) Schottky contact revealing good rectifying characteristics is a pivotal element. While forming metal/GaN contacts, Fermi-level pinning (FLP) hinders to obtain the metal work function dependent barrier heights [4,5]. To alleviate such FLP effect existing at metal/GaN contacts, insertion of very thin ZnO interlayers (ILs) between metal and GaN has been studied [6,7]. For example, Janardhanam *et al*. used a sputtered Al-doped ZnO IL in Au/GaN Schottky diode, which revealed the improved rectifying characteristics [7].

Among various growth techniques for ZnO, atomic layer deposition (ALD) can provide low-temperature grown ZnO films along with its unique advantages of precise thickness control and high conformity [8,9] and thus, can form high quality IL in metal/GaN junctions. Jeon et al. grew ZnO films by ALD at 70-250°C and showed that the ZnO film grown below 90°C is suitable for active channel layers in transparent electronic devices because of its chemical stoichiometry [10]. Park et al. could increase the carrier concentration (N_D) of ZnO films from ~10^{14} to ~10^{19} cm^{-3} by decreasing the growth temperature from 46 to 141°C [11]. Choi et al. studied the encapsulation effect of ZnO/Al_2O_3 bilayer grown at 60-250°C and observed that the material properties such as film crystallinity, density, and transmittance could be systematically modulated [12]. This indicates that ALD grown ZnO ILs are possibly incorporated into the fabrication process of GaN-based devices that requires low thermal budget. However, these works mainly characterized the film quality of ZnO layers. Still now, there is little knowledge regarding ALD-ZnO films grown below 100°C, in terms of the transport mechanisms governing the current flow across the MS interface. In this respect, we grew ZnO film on GaN at 80°C and investigated its effect on the Pt/GaN junction properties electrically.

2. Experimental

As a starting material, we used a undoped GaN (0001) substrate (thickness: 320 μm). This was loaded into a thermal ALD reactor (Atomic Shell, CN-1, Korea) after removing the native oxide by using $HCl:H_2O$ (1:1) solution. For ZnO growth at 80°C, diethyl zinc (DEZn: $Zn(C_2H_5)_2$) as the Zn precursor and H_2O as the oxygen reactant were utilized. As ALD pulse cycle, DEZn and H_2O were pulsed for 0.2 and 0.1 s, respectively, followed

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by N_2 purging for 15 s. The film thickness of ZnO was estimated to be 20 nm by a multi-wavelength spectroscopic ellipsometer (FS-1, Film Sense, USA). Using a radio-frequency magnetron sputter (Cryovac, Woosin, Korea), circular top Pt Schottky contacts (thickness: 50 nm, diameter: 500 μm) and Al back contact (thickness: 100 nm) were deposited on the front and back surfaces, respectively, to fabricate Schottky junctions. Using a Keithley 238 current source, the current–voltage–temperature (*I–V–T*) characteristics were measured with the voltage range of –2 V and +1 V, where the sample was placed on a hot chuck connected with a temperature controller. The capacitance–voltage (*C–V*) method was utilized with an HP 4284A LCR meter (ac voltage: 30 mV).

3. Results and discussion

Fig. 1(a) shows the experimental current density–voltage (*J–V*) data measured in the temperature range of 298-450 K. The forward current values increased with the temperature whereas the reverse current varied marginally. The forward current values were analyzed using the thermionic emission (TE) model to obtain the barrier height (Φ_B^{I-V}) and the ideality factor (n) [13]. As shown in Fig. 1(b), Φ_B^{I-V} increased and n decreased with the temperature, indicating the presence of inhomogeneous Schottky barrier [14]. Assuming a Gaussian distribution for the barrier height at Schottky contacts, the temperature dependences of Φ_B^{I-V} and n, are given as follows [14]

$$\Phi_B^{I-V} = \bar{\Phi}_B - \frac{q\sigma_0^2}{2kT} \tag{1}$$

$$\frac{1}{n} - 1 = -\rho_2 + \frac{q\rho_3}{2kT} \tag{2}$$

where $\bar{\Phi}_B$ is the mean barrier height, σ_0 is the standard deviation of interfacial potential, and ρ_2 and ρ_3 are the voltage-dependences of $\bar{\Phi}_B$ and σ_0, respectively. The plot of Φ_B^{I-V} vs. $1/2kT$ in Fig. 2(a) shows a linear relationship, indicating that Eq. (1) describes well the temperature dependence of Φ_B^{I-V} and the σ_0 is almost constant in the measurement temperature range. The values of $\bar{\Phi}_B$ and σ_0 were obtained as 1.15 eV and 152 mV, respectively. The obtained σ_0 is not small compared to $\bar{\Phi}_B$, indicating again the presence of barrier inhomogeneity at the MS interface [15]. In addition, the plot of $(n^{-1}–1)$ vs. $1/2kT$ shown in Fig. 2(b) exhibited a linear relationship, which produced the voltage coefficients of ρ_2 and ρ_3 as 0.478 V and –0.42 mV, respectively. The positive value of ρ_2 indicates that the mean barrier height increased with the forward bias and the negative value of ρ_3 implies that the standard deviation decreased with the bias voltage, possibly related with the image-force lowering [14].

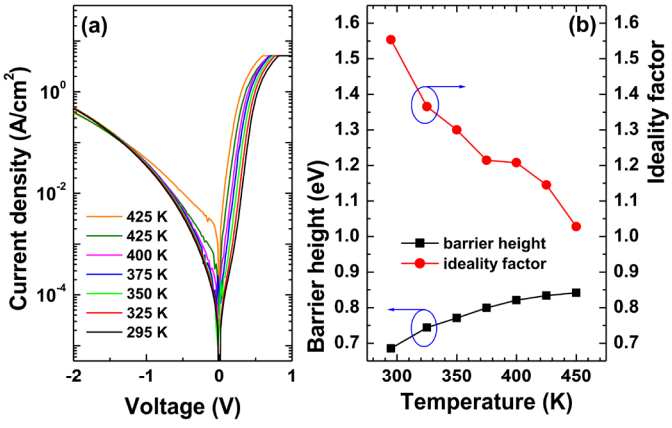

Fig. 1. (a) Current density–voltage (*J–V*) profiles at difference temperatures and (b) temperature dependences of barrier height and ideality factor

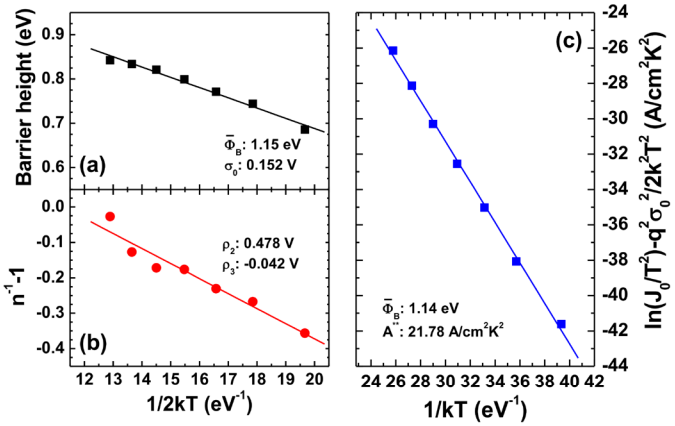

Fig. 2. Plots of (a) barrier height vs. $1/2kT$ and (b) $(n^{-1}–1)$ vs. $1/2kT$, and (c) modified Richardson plot

The conventional Richardson plot can be modified, with taking into account the inhomogeneous barrier, and is described as

$$\ln(J_0/T^2) - q^2\sigma_0^2/2k^2T = \ln(A^{**}) - \bar{\Phi}_B/kT \tag{3}$$

where J_0 is the reverse saturation current density and A^{**} is the Richardson constant. According to Eq. (3), the modified Richardson plot of $\ln(J_0/T^2) - q_2\sigma_0^2/2k^2T$ vs. $1/kT$ shown in Fig. 2(c) should be a straight line. From the linear fit to this plot, the value of $\bar{\Phi}_B$ was found to be 1.14 eV, almost same to the value obtained from Fig. 2(a). The intercept in the ordinate yielded the Richardson constant of 21.78 $Acm^{-2}K^{-2}$, similar to the theoretical value (26.4 $Acm^{-2}K^{-2}$ for n-GaN). This assures that the inhomogeneous barrier is involved in the forward *I–V* characteristics.

The *C–V* curve measured at 1 MHz is illustrated in Fig. 3(a). The built-in potential V_{bi} was calculated from the A^2/C^2 vs. V plot using the following equation [16]

$$\frac{A^2}{C^2} = 2\left(\frac{V_{bi} - V - kT/q}{qN_D\varepsilon_S\varepsilon_0}\right) \tag{4}$$

where A is the contact area and ε_S is the static dielectric constant (9.5 for GaN). After extracting N_D from the slope of the linear fit to A^2/C^2 vs. V plot as shown in Fig 3(b), the barrier height was deduced from $\Phi_B^{C-V} = qV_{bi} + qV_n$, where qV_n is the difference in energy between the conduction band (E_C) and the Fermi level (E_F). The value of Φ_B^{C-V} was calculated to be 1.13 eV. This is

similar to $\overline{\Phi}_B$ but is higher than Φ_B^{I-V}, attributed to the nonuniform interfacial layer and nonuniformly distributed interfacial charges that induce barrier inhomogeneity [17].

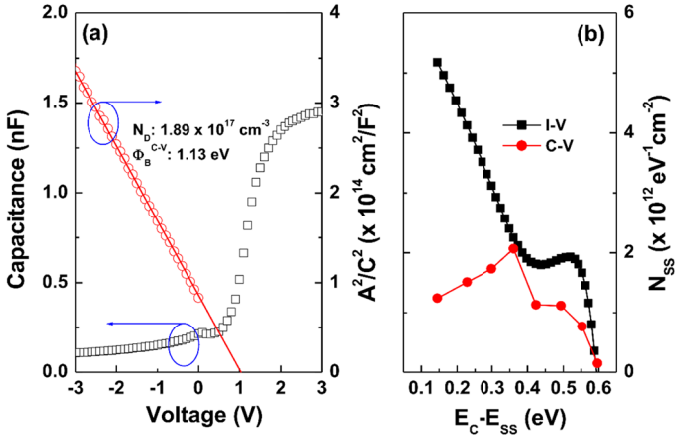

Fig. 3. (a) Capacitance–voltage (*C–V*) curve measured at 1 MHz and plot of A^2/V^2 vs. voltage and (b) interface state density (N_{SS}) vs. energy level (E_C–E_{SS})

The distribution of the interface state density (N_{SS}) is connected with the bias-dependent ideality factor, $n(V) = qV/[kT\ln(J/J_0)]$, as follows [18]

$$N_{SS}(V) = \frac{1}{q}\left[\frac{\varepsilon_i\varepsilon_0}{\delta}(n(V)-1) - \frac{\varepsilon_S\varepsilon_0}{W_D}\right] \tag{5}$$

where ε_i, and W_D are the dielectric constant of the interfacial layer (thickness: δ) and the depletion layer width (76.0 nm in this work), respectively. The value of $\varepsilon_i\varepsilon_0/\delta$ was selected as the capacitance in the accumulation region. The energy level, E_C–E_{SS} is related with the voltage-dependent effective barrier height, $\Phi_e = \Phi_B^{I-V} + (1 - 1/n(V))(V - IR_S)$ (R_S: series resistance) through the equation $E_C - E_{SS} = q(\Phi_e - V)$. The N_{SS} values were also estimated from the *C–V* measured values. The diode capacitance is dependent on the frequency as follows [17]. At low frequency, interface states can respond to the ac signal and the diode capacitance is given as the combination of the space-charge capacitance (C_{SC}) and the interface state capacitance (C_{SS}) ($C_{LF} = C_{SC} + C_{SS}$). Whereas, the charges on the interface states cannot follow the high-frequency ac signal and thus, the diode capacitance is equivalent with the space-charge capacitance ($C_{HF} = C_{SC}$). Then, N_{SS} can be determined as $N_{SS} = (C_{LF} - C_{HF})/qA$, where C_{LF} and C_{HF} are low- and high-frequency *C–V* measured values, respectively (in this work: 5 kHz and 1 MHz). The N_{SS} values from *C–V* values were lower than those from *I–V* values, as shown in Fig. 3(b). When the interface states are localized across the current paths, *I–V* measurement can produce an estimation of local N_{SS} over the contact areas. In contrast, *C–V* measurement produces the average value of N_{SS}. Therefore, such difference in N_{SS} might be associated with the nonuniformly distributed interface states, connected with the barrier inhomogeneity.

To search for the reverse current transport property, the reverse current density $\ln(J_R)$ vs. voltage $(V_R)^{1/2}$ was calculated. When the reverse *I–V* is governed by the Poole–Frenkel emission (*PFE*), it is described as [19]

$$J_R = J_0 \exp\left(\frac{\beta_{PF}V^{1/2}}{kTd^{1/2}}\right) \tag{6}$$

where β_{PF} is PFE coefficient and d is the film thickness. Considering the high-frequency dielectric constant of 5.35 for GaN [20], the theoretical value of β_{PF} for GaN is given as 3.28×10^{-4} eVV$^{-1/2}$ cm$^{1/2}$. Fitting results with the *PFE* model is shown in Fig. 4(a). The obtained values of β_{PFE} for each temperature are relatively higher than the theoretical one. To explain such difference, Gould and Bowler employed the modified PFE model [21], in which the enhanced β_{PF} is attributed to the localized electric fields existing near the traps. During the ALD process, the interfacial stress might cause structural defects and point defects such as Zn interstitials and oxygen vacancies might introduce non-stoichiometric growth of ZnO films. Hence, high density of trap states might be formed near the ZnO/GaN interface. These interface traps could lower the potential barriers with applied bias voltage and thereby increased the reverse leakage current.

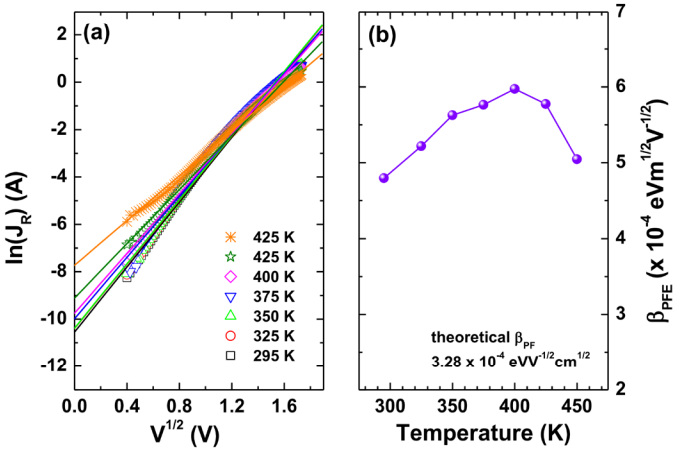

Fig. 4. (a) Fitting results for the reverse leakage current data with the Poole Frenkel emission (*PFE*) model and (b) obtained *PFE* coefficients at each temperature

4. Conclusions

The electrical characteristics of Pt/ZnO/GaN heterojunctions were examined after growing ZnO film at 80°C by thermal ALD. The analysis on the *I–V* characteristics suggested that the junction had inhomogeneous Schottky barrier. The values of N_{SS} extracted from *I–V* method were higher than those from *C–V* method, probably due to the nonuniformly distributed interface states. The larger *PFE* coefficient than the theoretical one was observed, implying the presence of high density of interface states. These results suggest that reducing the density of these trap states is a key factor to improve the properties of Pt/GaN contact with a low-temperature grown ZnO IL.

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